Commercializing Medium Voltage VFD that Utilizes High Voltage SiC Technology

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***Abstract*— This paper discusses system level challenges faced in designing and commercializing a Variable Frequency Drive (VFD) system utilizing high speed, high voltage, and high power density switching devices that incorporate Silicon Carbide (SiC) MOSFET technology.**

Keywords — VFD; SiC; Medium Voltage; High Efficiency; dv/dt (rate of change of voltage); di/dt (rate of change of current)

I. INTRODUCTION

The SiC device based inverter technology will allow for higher switching frequencies when compared to the existing silicon (Si) technology. Increasing switching frequency has several advantages, such as eliminating filter inductors, driving high rpm machines, and lowering rotor eddy current losses [1]. The lower loss SiC inverter also will enable use of higher temperature cooling media at a given switching frequency compared to Si devices.

Medium Voltage (MV) high power motor drives are popular in oil & gas, mines, power stations, and metal processing plants, as they operate at higher supply voltages to obtain lower losses and use smaller cables that add up to improved overall drive efficiency. This attribute contributes to lower system cost, especially when the distance between the VFD and motor is very long due to environmental and application requirements. Si based devices are typically used for MV drives due to availability and because of the maturity of the technology. However, high switching losses of Si devices, such as insulated gate bipolar transistors (IGBT), prevent it from being used in very high speed motor drive applications, which require higher switching frequencies.

Power switching devices using SiC technology have been widely used in high performance motor drives due to their high breakdown voltage, high operating temperature, and high switching frequency, leading to designs with high efficiency and power density [2-4]. However, there are many challenges to overcome when designing Medium Voltage drive systems using high voltage SiC devices.

In the first section of this paper, we present some of the key tests and performance analyses of a low voltage SiC MOSFET based VFD in comparison with a Si IGBT based VFD. For this exercise, we used a 125 KW low voltage Calnetix standard Vericycle™ 300 drive, where the motor inverter was initially tested in its standard form using a Si device. Then, the Si device was replaced by a SiC device and the tests were repeated.

In the second section, we will discuss the challenges involved in the system design and commercialization of a 10 kV 1MW Medium Voltage VFD using SiC technology.

II. LOW VOLTAGE SIC MOSFET TESTS AND COMPARISON

A. *Typical Calnetix Hardware Architecture of VFD with Active Front End*

Fig. 1 shows the simple VFD power architecture, which consists of two identical inverter modules interconnected by a DC link capacitor. The DC link capacitor provides a low voltage ripple DC energy buffer for the modules. Both modules are similar in construction and configuration and therefore are capable of bidirectional power flow operation (motoring mode or generating mode). All Calnetix VFDs are configured for bidirectional operation as applications require both motoring and grid-tie support. The nominal DC link voltage is 750 volts, which can provide three phase 480 volts at the input as well as the output. The continuous power rating of the VFD is 125 kW. Both grid and motor inverters are controlled by two independent controllers. The inverter control uses a Calnetix proprietary sensor-less control algorithm based on field oriented space vector topology.

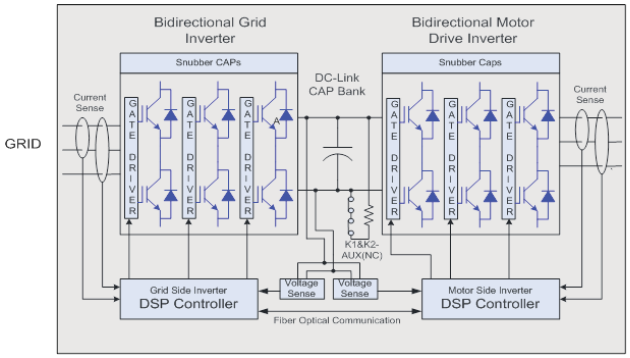

Fig. 1. Typical power architecture of VFD with active front end.

The baseline rated power performance test was conducted on an existing Si IGBT (FF900R12IE4) based inverter mounted on a single liquid cooled heat exchanger. After completing the baseline test, the motor inverter was re-packaged with a SiC based MOSFET (CAS300M12BM2) with smaller liquid cooled heat exchanger. The results were tabulated and compared for efficiency performance. Fig. 2 shows the original 125 kW power module with the existing Si device. Fig. 3 shows the modified 125 kW power module with SiC device.

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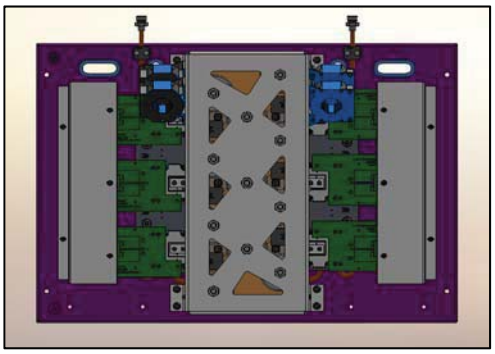

Fig. 2. 125kW power module with existing Si device.

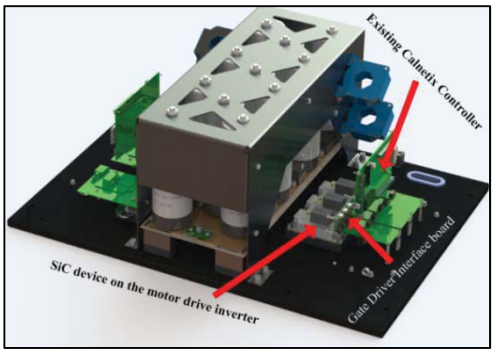

Fig. 3. Modified 125kW power module with SiC device.

B. Heat Run Test

The heat run test was performed to compare the losses between two configurations. A 200 Amp rms passive inductive load was used to drive the inverter. The test conditions and the water temperatures after thermal stabilization are tabulated in Table I.

TABLE I. TEST CONDITIONS AND STEADY STATE TEMPERATURE

Parameter	Device Type	
	Si-IGBT	***SiC-MOSFET***
DC bus voltage	750 V	
Fundamental frequency	500 Hz	
Switching frequency	8.15 kHz	
Output current	200 Arms	
Cooling water pressure	55 kPa (8 PSI)	
Cooling water flow rate	1.5 GPM	1.4 GPM
Water inlet temperature	31.4 °C	24.6 °C
Water outlet temperature	36.2 °C	26.7 °C
Water temperture delta	4.8 °C	2.1 °C

The heat transfer by the water can be calculated using the following heat balance equation:

$$P = Cp \times m \times dT \quad (1)$$

Where *Cp* is the specific heat of the water, *m* is the mass flow rate of the water, and *dT* is the temperature increase of the water.

Based on the heat balance equation, the calculated losses transferred by water are 1,900 W and 775 W for Si IGBT and SiC MOSFET respectively.

The simulated losses, based on manufacturer tools, for the same running condition are tabulated in Table II.

TABLE II. SIMULATION RESULTS

Parameter	Device Type	
	Si-IGBT	***SiC-MOSFET***
Conduction loss	594 watts	653 watts
Switching loss	2140 watts	235 watts
Total loss	2734 watts	888 watts

Our estimate is that approximately 75 - 85% of the heat losses are coupled through the heat exchanger considering that some heat losses are removed by natural convection. The test results and the simulation results match closely. These results indicate that the SiC devices improve the inverter efficiency significantly by virtue of their considerably lower switching losses.

C. Switching Data

The switching dv/dt of the SiC MOSFET inverter is much higher than the Si IGBT inverter. For the same running condition, turn-off Vce voltage of both the Si IGBT and the SiC MOSFET configurations were measured and the results are shown in Fig. 4 and Fig. , respectively. Fig. 5 shows SiC turn-off without the optimization of the gate driver and snubber circuits. The initial dv/dt measurement was >12,000 V/µsec and the overshoot exceeded the voltage rating of the device. Fig. 6 shows the turn-off after optimizing the gate resistors, snubber circuit and minimizing the bus inductance.

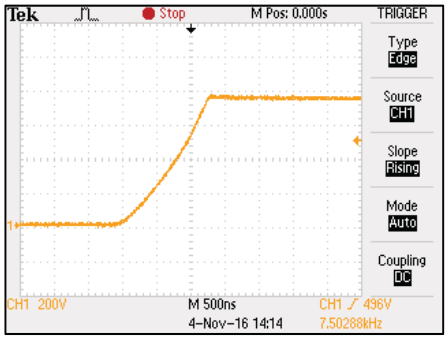

Fig. 4. Turn-off Vce voltage of Si IGBT (600 v/µsec).

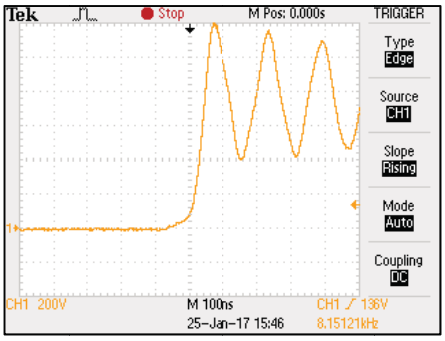

Fig. 5. Turn-off Vce voltage of SiC MOSFET (>12,000 v/µsec)

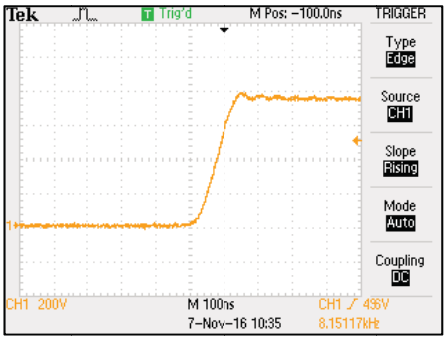

Fig. 6. Turn-off Vce voltage of SiC MOSFET (6,200 v/µsec).

III. Medium Voltage VFD System Design and Challenges

When this paper was written, the Medium Voltage inverter was in design phase, and therefore, the paper only discusses the design steps followed based on some of the lessons learned from the low voltage SiC MOSFET tests. The expected test start date of a half bridge inverter is in late Q2, 2017.

The inverter topology is based on a simple two level architecture using a dual 10 kV SiC package manufactured by Cree Fayetteville Inc., a company that specializes in high density and high power electronic solutions and products based on new and emerging materials, such as SiC. Fig. 7 shows the module outline, which is rated for 10 kV, 270 Amps at 25°C case temperature. The module is very compact with overall dimensions of 195 mm width, 125 mm depth, and 23.5 mm height.

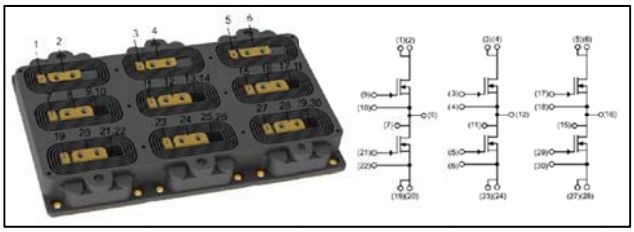

Fig. 7. Cree 10 kV XHV-6 module.

Based on our ongoing design and fabrication efforts, we have identified the following challenges and design considerations:

- Low impedance bus work, snubber design and managing high rate of change of voltage (dv/dt).
- Selecting and sourcing filter components, such as inductors and capacitors.
- Impact and mitigation of high dv/dt impressed on motor stator insulation system.
- Managing motor bearing currents due to high dv/dt.
- Implementation of robust controls.
- Packaging to address EMI/EMC issues due to high dv/dt.

Fig. 8 shows one leg of a three phase MV inverter assembly using a 10 kV SiC module. The design is extremely compact with laminated dc bus bars to minimize the total bus inductance. Three such assemblies are required to build a three phase inverter.

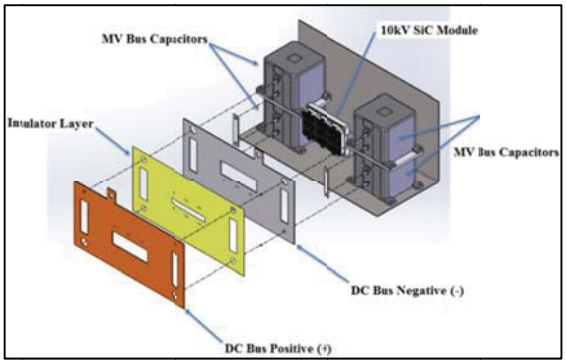

Fig. 8. 10 kV SiC Medium Voltage inverter assembly.

A. Low Impedance Bus Work and Snubber Design

Because of higher dv/dt and di/dt, the switching devices will see large over voltage transients if the circuit loop stray inductance is not minimized. To control the voltage overshoot within the safe value, the inductance of the circuit loop has to be minimized. To mitigate the voltage overshoot, a low inductance laminated bus-plate design was developed as shown in Fig. 8. In addition, a suitable snubber capacitor with low parasitic inductance will be used in parallel with the device. Based on our experience in developing the low voltage SiC inverter, the optimization of gate drive turn on and off resistors are also included in the design.

B. Selecting and Sourcing Filter Components (Inductors, Capacitors)

Filter capacitors include dc bus capacitors, which are used to reduce dc bus voltage ripple, and ac capacitors, which are used for dv/dt filter and/or sinusoidal filter at the inverter output. It is extremely important that the dc bus capacitors selected have low parasitic inductance and high di/dt rating.

Design of the filter inductor has multiple challenges. The filter inductor, which is between the inverter output and motor interface, is subjected to extremely high dv/dt of the SiC switching. Therefore, the filter inductor design needs to take into consideration the following:

- The inductor insulating system should be able to survive a large dv/dt.
- The parasitic capacitance of the inductor should be minimized. The parasitic capacitance will create a virtual short-circuit of the SiC device during switching.

Currently, several inductor options are being discussed with the manufacturer design group and prototypes are being developed for evaluation. One approach is to construct the inductor in several smaller increments so the overall dv/dt and parasitic capacitor affects are minimized.

C. Managing (dv/dt) Impressed on Motor and Impact on Motor Operating Life

High dv/dt will reduce winding insulation lifetime and cause premature insulation failure. For the Medium Voltage motor winding, maintaining the winding turn to turn voltage below 50-75V and reducing the impressed dv/dt will improve the insulation life. Typical Medium Voltage insulation systems are rated for soft dv/dt, typically less than 2000 v/μsec.

There are filter options that have been evaluated and include the following:

- A sinusoidal filter, which is very effective but will increase the inverter current, reduces operating efficiency and increases the cost and size due to bulky capacitors [4].
- A simple inductance capacitance (LC) filters to reduce dv/dt just to soften the leading edge of the waveform.

Currently, the second option of using an LC filter is being evaluated.

D. Implementation of Controls and Protection

The VFD controller needs to be very robust primarily when subjected to a high dv/dt switching environment. The Calnetix controller has been successfully evaluated in a low voltage SiC inverter. The expected dv/dt in the Medium Voltage inverter system is six times higher than that impressed in the low voltage inverter. The controller is housed in a sealed cage to minimize the impact of radiated EMI and incorporates a fiber optic gate driver interface as suggested by the SiC device manufacturer. To minimize high frequency circulating ground currents, design considerations must be given to a single point grounding scheme.

E. Managing Motor Bearing Currents due to High dv/dt

Circulating bearing currents in motors due to high voltage and associated dv/dt caused by PWM switching has been a known phenomenon [5].

An LC filter recommended in section C will minimize the bearing current but does not eliminate the occurrence entirely. Calnetix recommends the use of magnetic bearings as another option to conventional bearings as the use of magnetic bearings eliminates the inherent contact between the rotor and the static components and/or motor housing.

F. EMI/EMC Issue due to High dv/dt Packaging

Because of high dv/dt, the packaging design to minimize EMI/EMC issues becomes very important. Random control failure or interrupted internal or external communication can occur if the packaging is not properly addressed. Some of the key improvements considered include:

- Use of EMI gaskets around the door and panels.
- Completely enclosed controls preferably in a metal enclosure.
- An optically isolated drive interface from the controller to the drive board as well as any external communication cables.
- Use of proper high frequency shielded control cables.

IV. Conclusion

The most important commercial aspect of an industrial VFD is its price. As of today, the SiC MOSFET device cost is considerably higher than its Si IGBT counterpart. The additional system cost and challenges associated in managing the high switching dv/dt cannot be ignored. SiC devices offer a definite performance advantage due to their ability to switch at higher frequency with reduced switching losses, but unless the price of the SiC device comes close to its counterpart, it is challenging to justify these devices in industrial applications. It is our perception that as the SiC devices are adopted in various applications that the device cost will reduce significantly and allow for full adoption of SiC devices and replace Si devices altogether.

However, if the price is secondary and the design requires > 600V, SiC is the device of choice for high switching frequency to control very high speed machines with low current harmonics, small size and footprint, and high efficiency.

Acknowledgment

This development work is supported by Department of Energy (DOE) under Award No. DE-EE0007251, where Calnetix is in process of developing a > 1 MW at > 15,000 RPM motor and VSD that will demonstrate the commercial viability of wide band gap power electronics for use with MW class motors. Partners for this project include Cree Fayetteville Inc. and their 10 kV SiC module and corresponding gate drive board, and CTM Magnetics and their custom LC filter design.

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